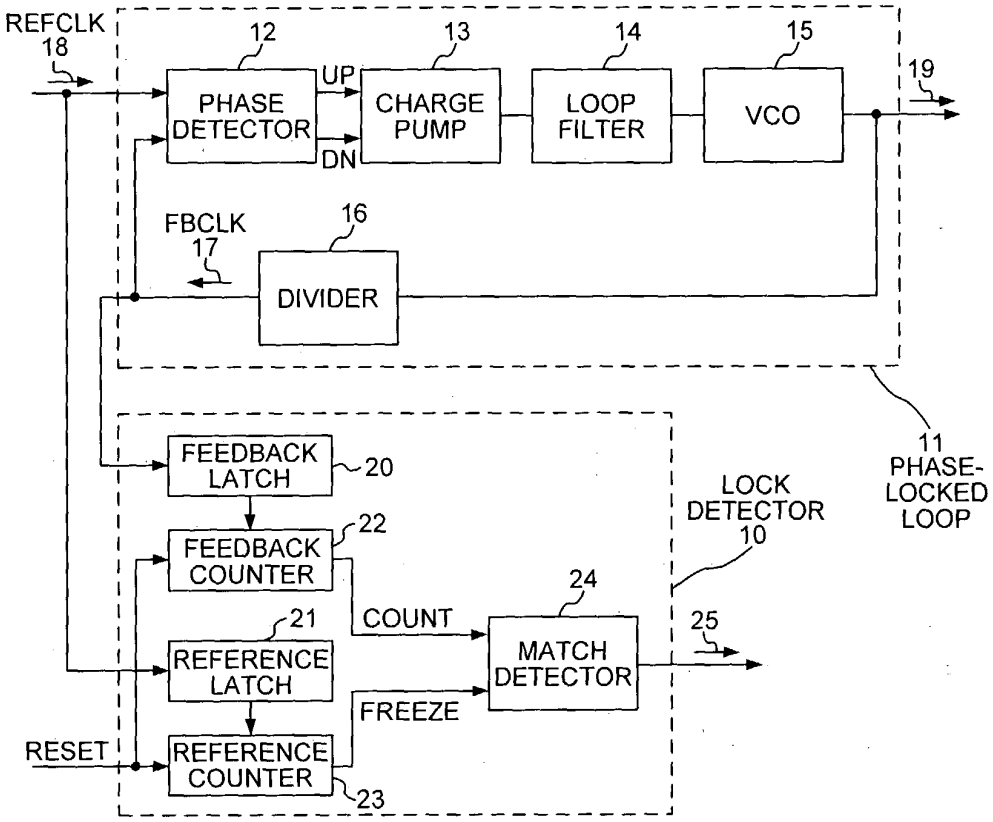

FIG. 1
(PRIOR ART)

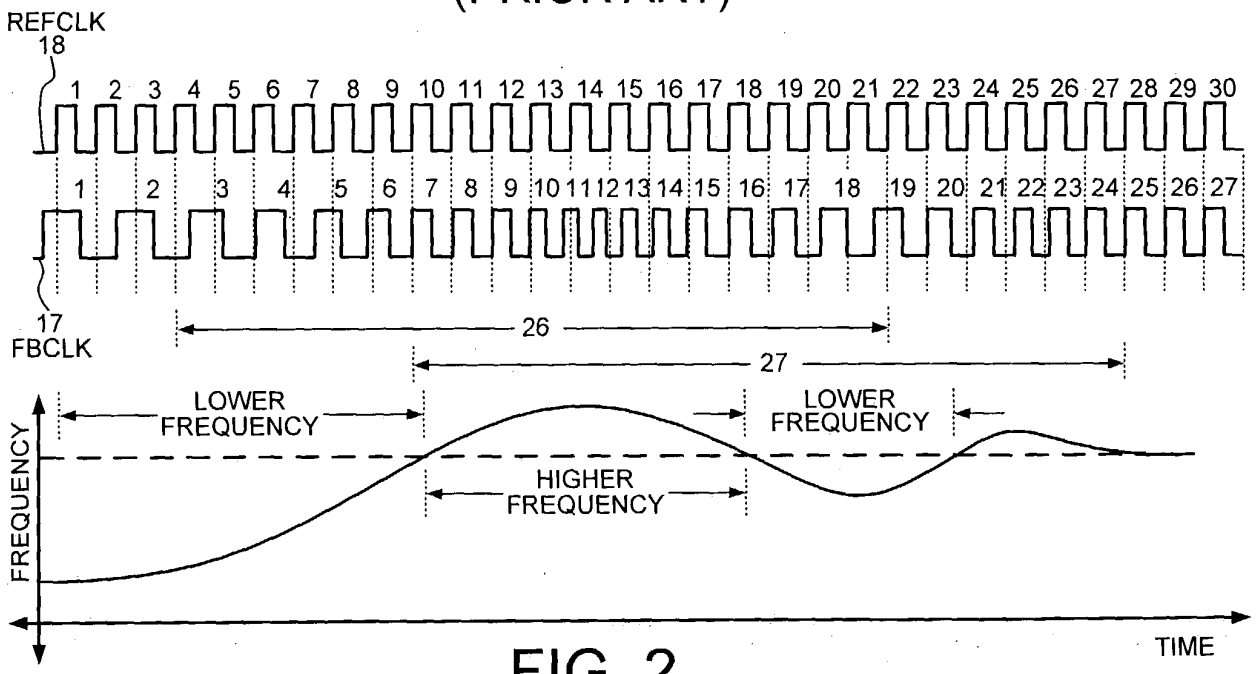

FIG. 2
(PRIOR ART)

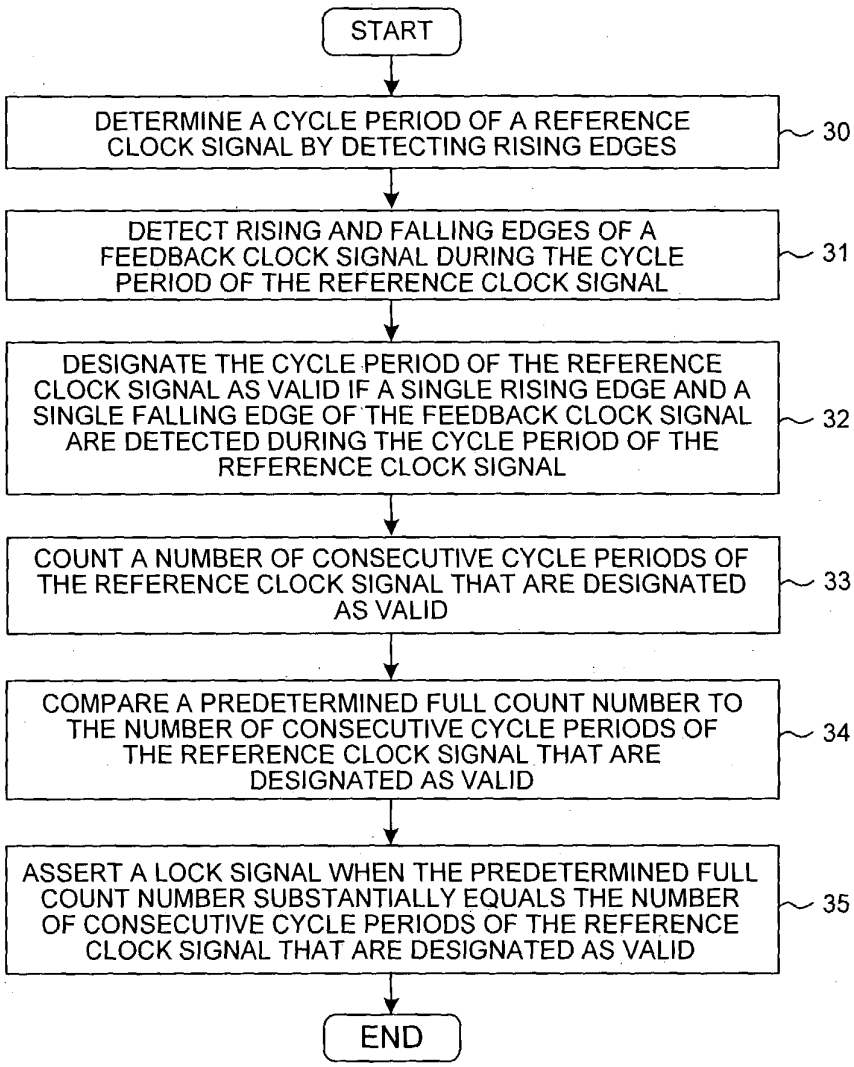
START
DETERMINE A CYCLE PERIOD OF A REFERENCE CLOCK SIGNAL BY DETECTING RISING EDGES
30
DETECT RISING AND FALLING EDGES OF A FEEDBACK CLOCK SIGNAL DURING THE CYCLE PERIOD OF THE REFERENCE CLOCK SIGNAL
31
DESIGNATE THE CYCLE PERIOD OF THE REFERENCE CLOCK SIGNAL AS VALID IF A SINGLE RISING EDGE AND A SINGLE FALLING EDGE OF THE FEEDBACK CLOCK SIGNAL ARE DETECTED DURING THE CYCLE PERIOD OF THE REFERENCE CLOCK SIGNAL
32
COUNT A NUMBER OF CONSECUTIVE CYCLE PERIODS OF THE REFERENCE CLOCK SIGNAL THAT ARE DESIGNATED AS VALID
33
COMPARE A PREDETERMINED FULL COUNT NUMBER TO THE NUMBER OF CONSECUTIVE CYCLE PERIODS OF THE REFERENCE CLOCK SIGNAL THAT ARE DESIGNATED AS VALID
34
ASSERT A LOCK SIGNAL WHEN THE PREDETERMINED FULL COUNT NUMBER SUBSTANTIALLY EQUALS THE NUMBER OF CONSECUTIVE CYCLE PERIODS OF THE REFERENCE CLOCK SIGNAL THAT ARE DESIGNATED AS VALID
35
END

FIG. 3

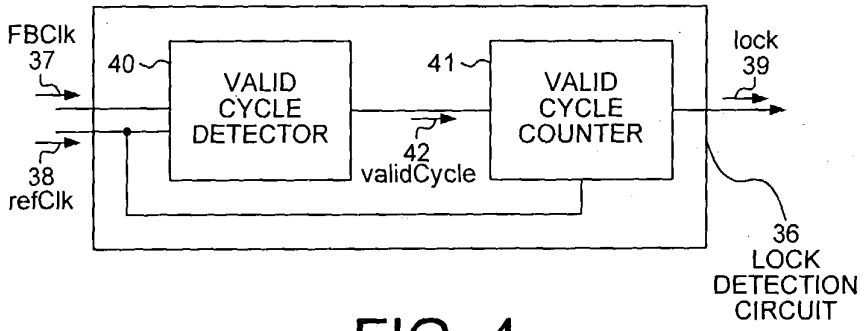
FBClk
37
40
VALID CYCLE DETECTOR
41
VALID CYCLE COUNTER
lock
39
42
validCycle
38
refClk
36
LOCK DETECTION CIRCUIT

FIG. 4

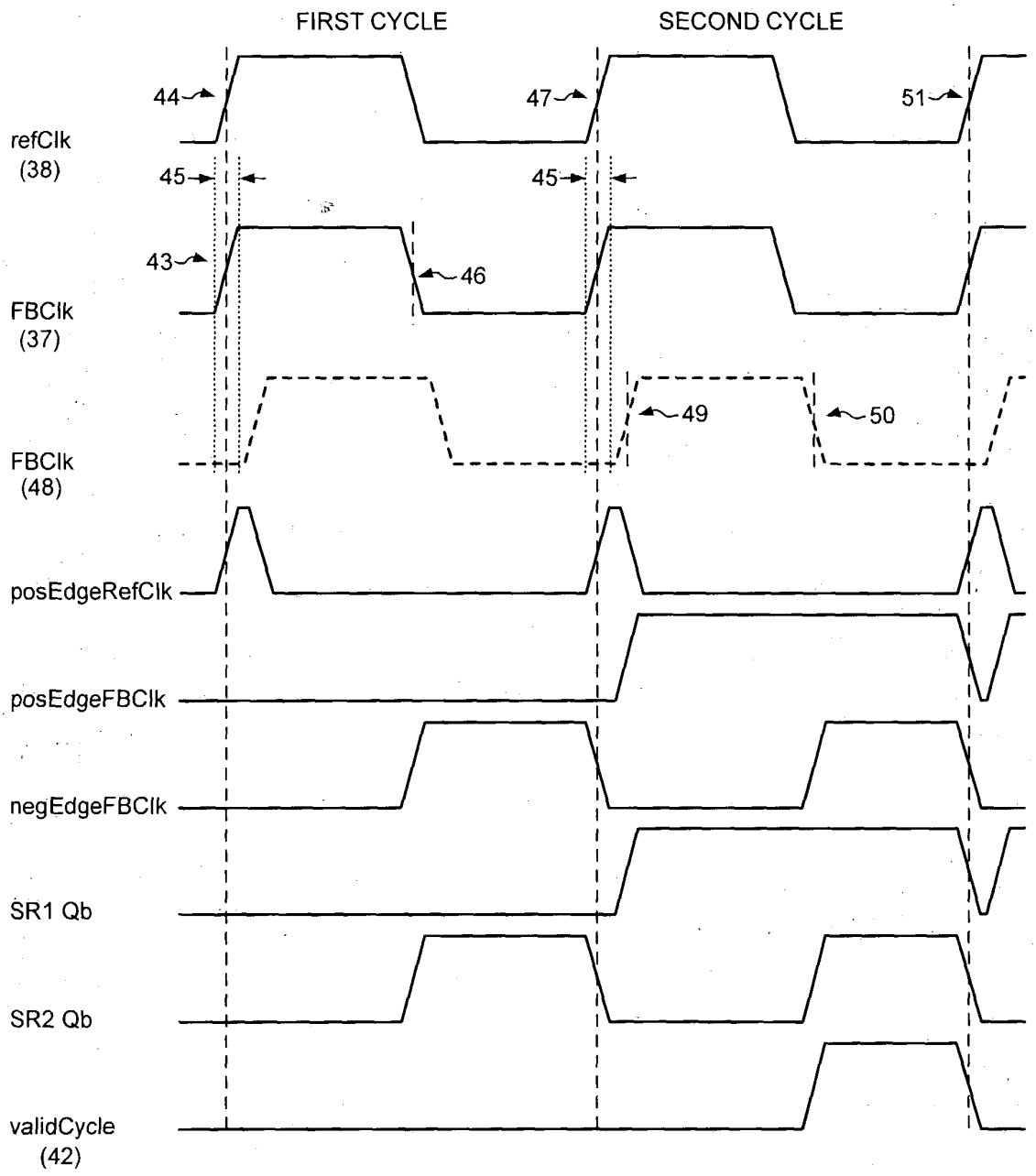
FIRST CYCLE
SECOND CYCLE
44
47
51
refClk
(38)
45
45
43
46
FBClk
(37)
49
50
FBClk
(48)
posEdgeRefClk
posEdgeFBClk
negEdgeFBClk
SR1 Qb
SR2 Qb
validCycle
(42)

FIG. 5

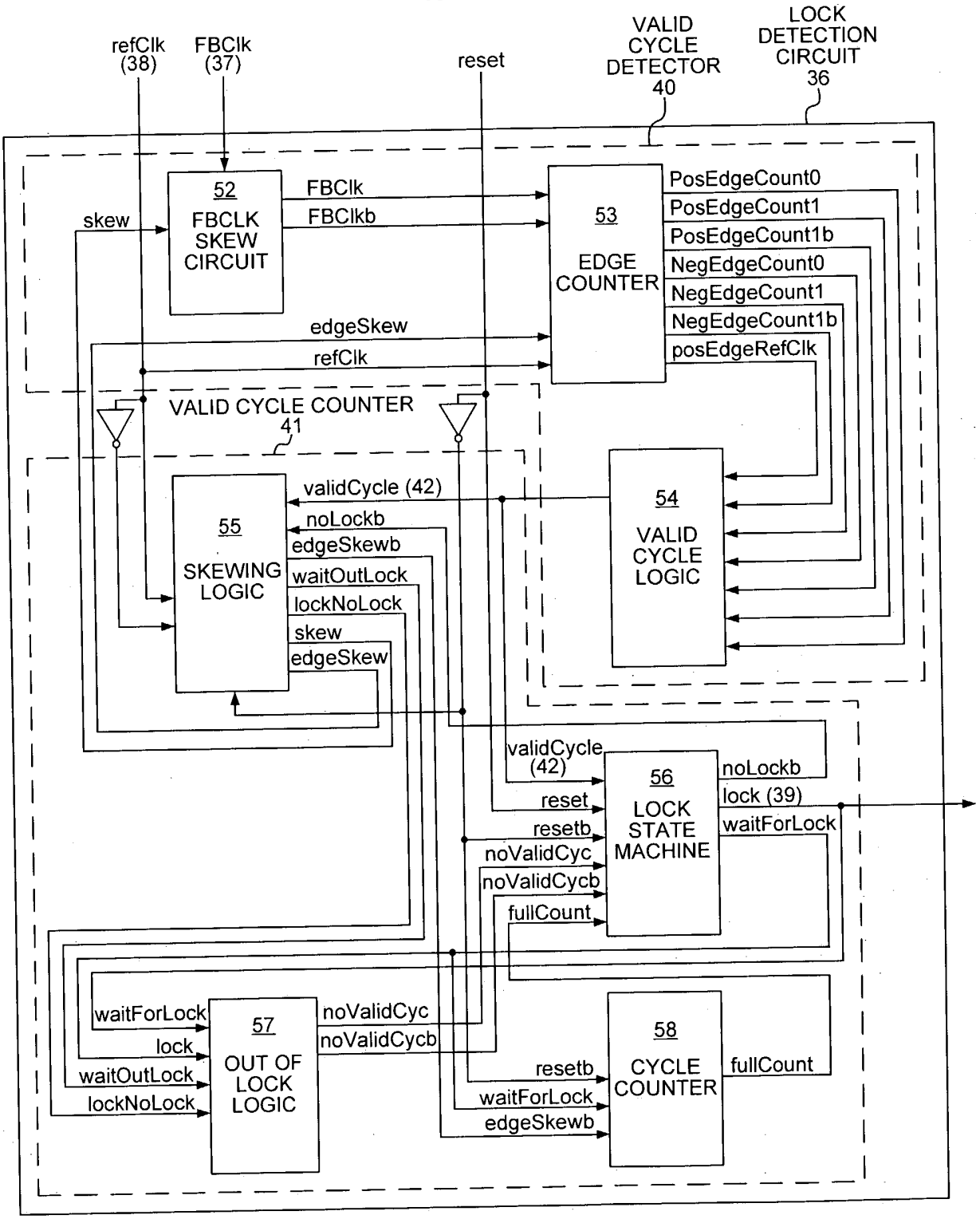
refClk (38)
FBClk (37)
reset
VALID CYCLE DETECTOR 40
LOCK DETECTION CIRCUIT 36
52 FBCLK SKEW CIRCUIT
skew
FBClk
FBClkb
53 EDGE COUNTER
PosEdgeCount0
PosEdgeCount1
PosEdgeCount1b
NegEdgeCount0
NegEdgeCount1
NegEdgeCount1b
posEdgeRefClk
edgeSkew
refClk
VALID CYCLE COUNTER 41
validCycle (42)
noLockb
edgeSkewb
waitOutLock
lockNoLock
skew
edgeSkew
55 SKEWING LOGIC
54 VALID CYCLE LOGIC
validCycle (42)
reset
resetb
noValidCyc
noValidCycb
fullCount
56 LOCK STATE MACHINE
noLockb
lock (39)
waitForLock
waitForLock
lock
waitOutLock
lockNoLock
57 OUT OF LOCK LOGIC
noValidCyc
noValidCycb
resetb
waitForLock
edgeSkewb
58 CYCLE COUNTER
fullCount

FIG. 6

STATES OF VALID CYCLE COUNTER

CURRENT STATE	INPUT SIGNALS	waitOutLock SIGNAL	NEXT STATE	OUTPUT VALUES
0 0 1	0 0 0	X	0 0 1	0 0 1
0 0 1	0 0 1	X	0 0 1	0 0 1
0 0 1	0 1 0	X	0 1 0	0 0 1
0 0 1	0 1 1	X	0 1 0	0 0 1
0 0 1	1 0 0	X	0 0 1	0 0 1
0 0 1	1 0 1	X	0 0 1	0 0 1
0 0 1	1 1 0	X	0 1 0	0 0 1
0 0 1	1 1 1	X	0 1 0	0 0 1
0 1 0	0 0 0	X	0 1 0	0 1 0
0 1 0	0 0 1	X	NOT POSSIBLE	0 1 0
0 1 0	0 1 0	X	NOT POSSIBLE	0 1 0
0 1 0	0 1 1	X	NOT POSSIBLE	0 1 0
0 1 0	1 0 0	X	1 0 0	0 1 0
0 1 0	1 0 1	X	NOT POSSIBLE	0 1 0
0 1 0	1 1 0	X	NOT POSSIBLE	0 1 0
0 1 0	1 1 1	X	NOT POSSIBLE	0 1 0
1 0 0	0 0 0	0	1 0 0	1 0 0
1 0 0	0 0 1	0	1 0 0	1 0 0
1 0 0	0 1 0	0	NOT POSSIBLE	1 0 0
1 0 0	0 1 1	0	NOT POSSIBLE	1 0 0
1 0 0	1 0 0	0	1 0 0	1 0 0
1 0 0	1 0 1	0	0 0 1	1 0 0
1 0 0	1 1 0	0	NOT POSSIBLE	1 0 0
1 0 0	1 1 1	0	NOT POSSIBLE	1 0 0
1 0 0	0 0 0	1	0 1 0	1 0 0
1 0 0	0 0 1	1	0 1 0	1 0 0
1 0 0	0 1 0	1	NOT POSSIBLE	1 0 0
1 0 0	0 1 1	1	NOT POSSIBLE	1 0 0
1 0 0	1 0 0	1	1 0 0	1 0 0
1 0 0	1 0 1	1	0 0 1	1 0 0
1 0 0	1 1 0	1	NOT POSSIBLE	1 0 0
1 0 0	1 1 1	1	NOT POSSIBLE	1 0 0

waitForLock noLock lock

validCycle (42) noValidCyc fullCount

waitForLock noLock lock

waitForLock noLock lock

FIG. 7

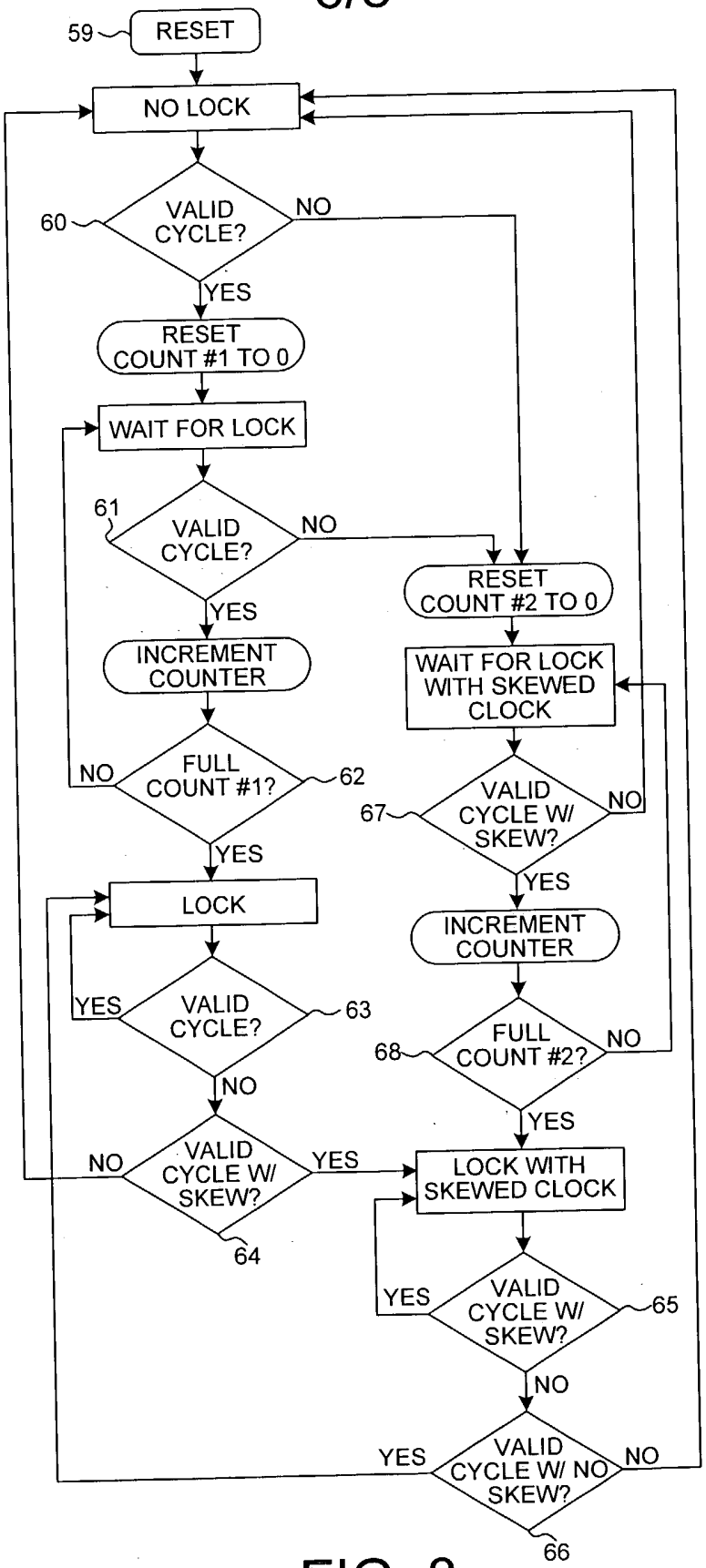
59
RESET
NO LOCK
60
VALID CYCLE?
NO
YES
RESET COUNT #1 TO 0
WAIT FOR LOCK
61
VALID CYCLE?
NO
YES
INCREMENT COUNTER
NO
FULL COUNT #1?
62
YES
LOCK
YES
VALID CYCLE?
63
NO
NO
VALID CYCLE W/ SKEW?
YES
64
RESET COUNT #2 TO 0
WAIT FOR LOCK WITH SKEWED CLOCK
67
VALID CYCLE W/ SKEW?
NO
YES
INCREMENT COUNTER
68
FULL COUNT #2?
NO
YES
LOCK WITH SKEWED CLOCK
YES
VALID CYCLE W/ SKEW?
65
NO
YES
VALID CYCLE W/ NO SKEW?
NO
66

FIG. 8

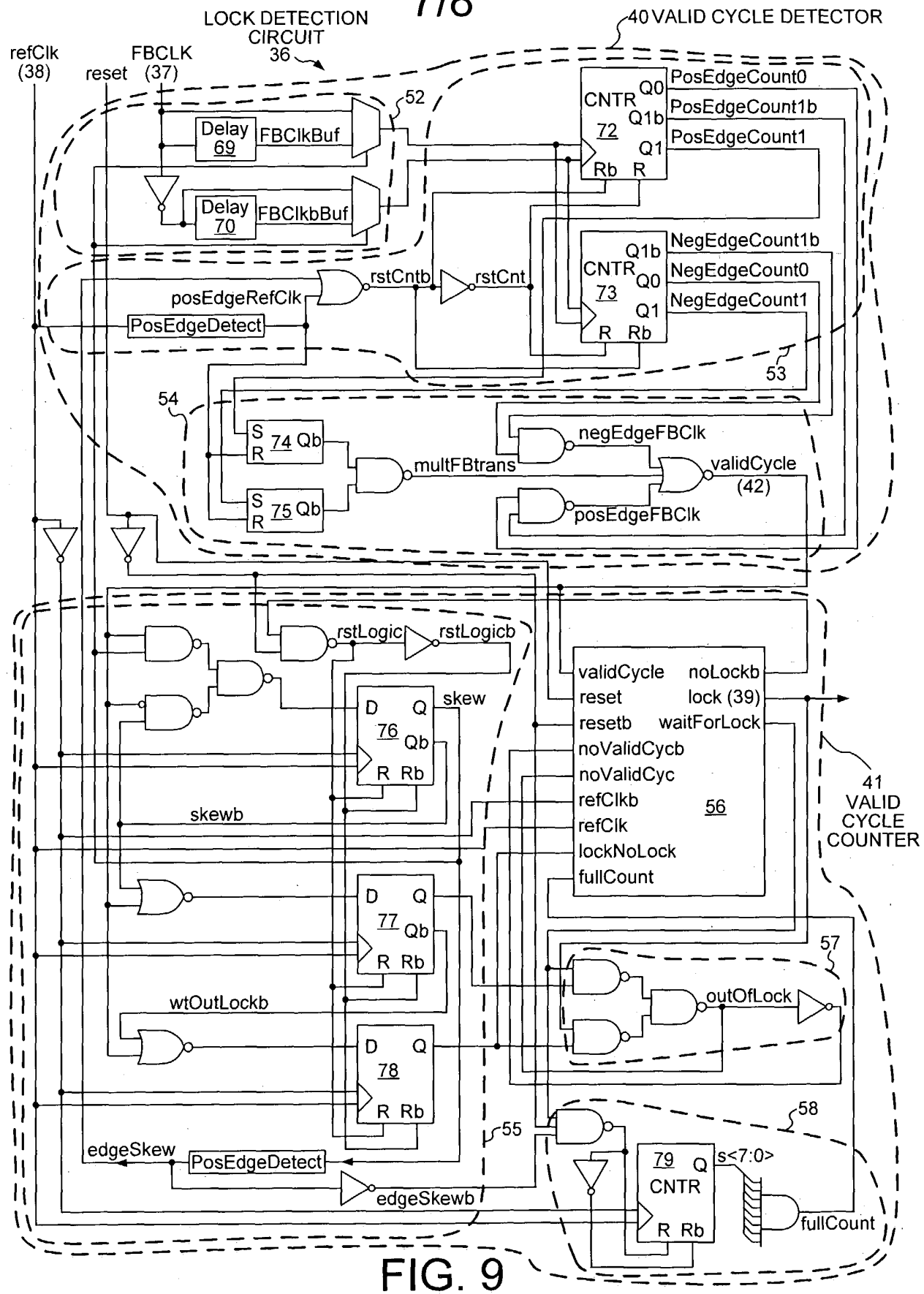
LOCK DETECTION CIRCUIT 36
40 VALID CYCLE DETECTOR
refClk (38)
reset
FBCLK (37)
52
Delay 69
FBClkBuf
Delay 70
FBClkbBuf
CNTR 72
Q0
Q1b
Q1
Rb R
PosEdgeCount0
PosEdgeCount1b
PosEdgeCount1
CNTR 73
Q1b
Q0
Q1
R Rb
NegEdgeCount1b
NegEdgeCount0
NegEdgeCount1
rstCntb
rstCnt
posEdgeRefClk
PosEdgeDetect
53
54
S R 74 Qb
S R 75 Qb
multFBtrans
negEdgeFBClk
posEdgeFBClk
validCycle (42)
rstLogic
rstLogicb
skew
D Q
76 Qb
R Rb
skewb
77
78
wtOutLockb
validCycle
reset
resetb
noValidCycb
noValidCyc
refClkb
refClk
lockNoLock
fullCount
noLockb
lock (39)
waitForLock
56
41 VALID CYCLE COUNTER
57
outOfLock
58
55
edgeSkew
PosEdgeDetect
edgeSkewb
79 Q
CNTR
R Rb
s<7:0>
fullCount

FIG. 9

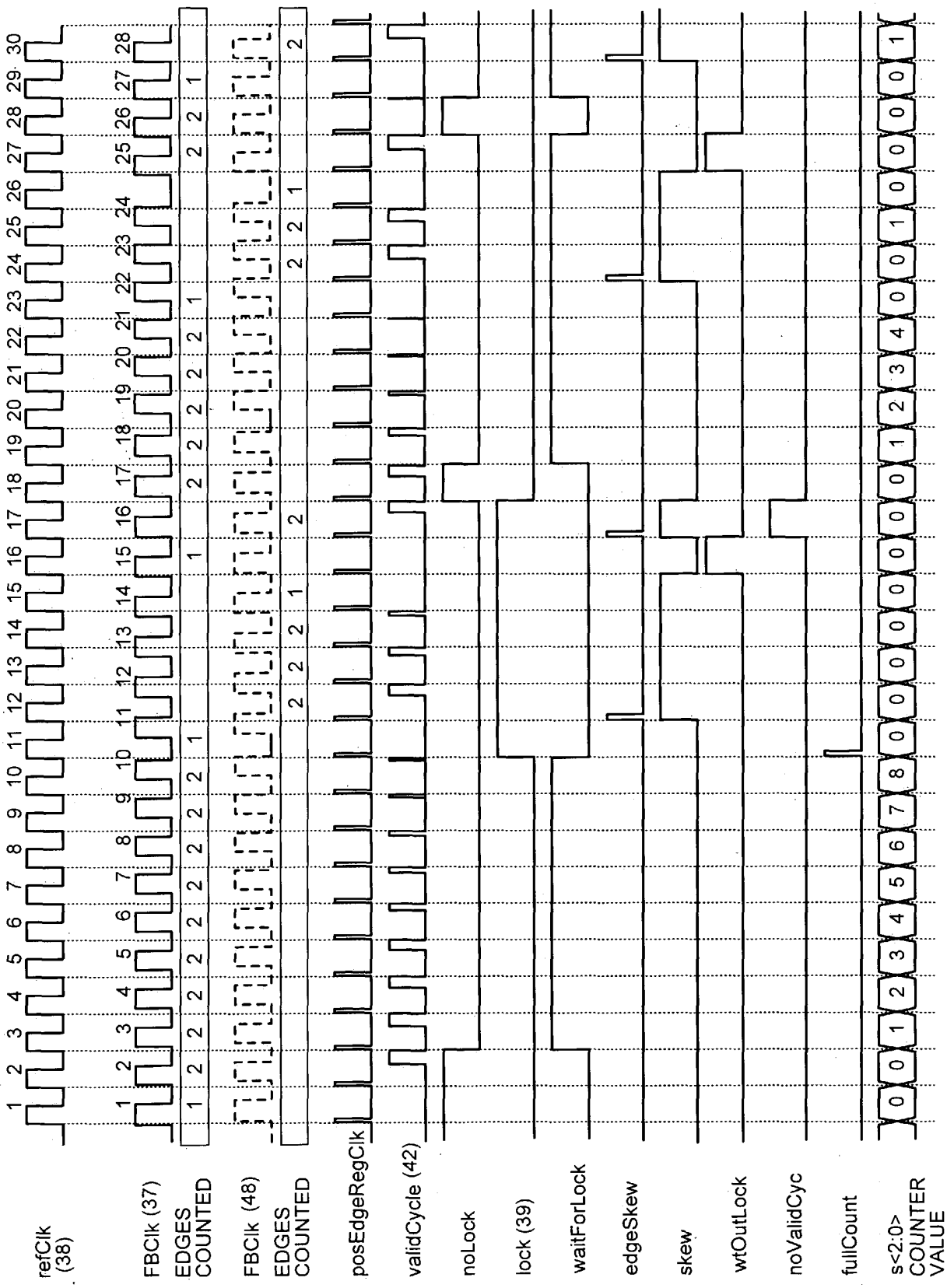
refClk (38)
FBClk (37)
EDGES COUNTED
FBClk (48)
EDGES COUNTED
posEdgeRegClk
validCycle (42)
noLock
lock (39)
waitForLock
edgeSkew
skew
wtOutLock
noValidCyc
fullCount
s<2:0> COUNTER VALUE

FIG. 10